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10/681,070	10/08/2003	Wayne Tran	ITL.1010US (P15535)	8625

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EXAMINER	
GOLDEN, JAMES R	

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/681,070	**Applicant(s)** TRAN ET AL.
	Examiner James Golden	**Art Unit** 2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,21-24 and 27-30* is/are rejected.

7)☒ Claim(s) *18-20,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *02/10/2004*.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

The instant application 10/681070 has a total of 30 claims pending. There are 4 independent claims and 26 dependent claims. Claims 1-17, 21-24 and 27-30 have been rejected in view of prior art. Claims 18-20 and 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Information Disclosure Statement

1. The information disclosure statement submitted on 02/10/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description: 10 of Fig. 1.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference characters not mentioned in the description: 332, 333, 334, 352, 382, 383 and 385 of Fig. 3.

4. The drawings are objected to because of the following informalities. 420 and 442 of Fig. 4 are described in the specification as 320 and 342 on page 18, line 24 and page

19, line 25, respectively. COMPARE 22 of Fig. 2 is described as 12 of Fig. 2 on page 12, line 13 and elsewhere. 221 of Fig. 2 is described as PFADDR 121 of Fig. 2 on page 15, line 13. PWR ON input 215 is described as PWRDN on page 11, line 15; DFDONE and FF1-FF3 of Fig. 3 are described as PFDONE and PF1-PF3 on page 17, line 17.

5. These lists of figures containing errors may not be exhaustive. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office Action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities: "the subject dynamic..." (page 3, line 10) should be corrected such that the title of the patent application is capitalized and in quotes; "now know" (page 13, line 11) should be corrected to --now known--. This list may not be exhaustive. Appropriate correction is required.

Claim Objections

7. **Claims 7-9, 17-20 and 22-23** are objected to because of the following informalities: "of a the second" (claim 7, line 10 and claim 8, line 5) should be corrected to --the second--; "a address" (claim 17, line 5) should be corrected to --an address--; "An system" (claim 22, line 1) should be corrected to --A system--; claims 9, 18-20 and 23 are objected to because of their dependence on claims 8, 17 and 22, respectively. These objections can be overcome by making the appropriate corrections.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. **Claims 1-17 and 27-30** are rejected under 35 U.S.C. 102(b) as being anticipated by Watkins (US 5,854,911).

10. **With respect to claim 1**, Watkins discloses a method determining whether a prefetched address is identical to a received address (abstract, lines 4-11).

11. **With respect to claim 2**, Watkins discloses a method as defined in claim 1 (see above paragraph 10) further comprising if the prefetched address is not to identical the received address, interrupting data transfer from a memory and applying the received address to the memory (column 6, lines 27-31).

12. **With respect to claim 3**, Watkins discloses a method as defined in claim 2 (see above paragraph 11), wherein determining whether the prefetched address is identical to the received address comprises: comparing the received address to the prefetched address using a comparator (column 6, lines 21-27).

13. **With respect to claim 4**, Watkins discloses a method as defined in claim 3 (see above paragraph 12), wherein the comparator is a gated comparator (the specification of the applicant notes, "Operation of COMPARE 22 is gated in the sense that its PFHIT output will be active only if the requisite PFVALID signal exists;" column 6, lines 15-31 of Watkins detail how the PFvalid signal will indicate a match, or become active, only when the PFvalid signal is active).

14. **With respect to claim 5**, Watkins discloses a method as defined in claim 4 (see above paragraph 13), wherein the comparator is enabled by a signal that assumes a predetermined logic level when prefetching of a respective prefetched address has been accomplished (PFvalid signal, column 6, lines 15-31, see above paragraph 13).

15. **With respect to claim 6**, Watkins discloses a method as defined in claim 3 (see above paragraph 12) wherein the comparator provides a first output when the

prefetched address is determined to be identical to the received address and a second output when the prefetched address is determined not to be identical to the received address (column 6, lines 24-31).

16. **With respect to claim 7**, Watkins discloses a method as defined in claim 6 (see above paragraph 15), further comprising:

- coupling the received address (rd_addr of Fig. 3; column 6, lines 56-59) to a first address input of a multiplexer (220 of Fig. 3; column 3, lines 44-48), the multiplexer having an output to couple to the memory (addr line connected to Address FIFO of Fig. 3);
- coupling the prefetched address to a second address input of the multiplexer (PF_addr of Fig. 3; column 6, lines 56-59);
- selecting the prefetched address in response to the first output from the comparator (column 6, lines 27-31); and
- selecting the received address in response to the second output from the comparator (column 6, lines 27-31).

17. **With respect to claim 8**, Watkins discloses a method as defined in claim 7 (see above paragraph 16), further comprising coupling the comparator output to the memory so that the data output of the memory is interrupted in response to the appearance of the second output signal at the comparator output ("execute a memory access cycle," column 6, lines 27-31).

18. **With respect to claim 9**, Watkins discloses a method as defined in claim 8 (see above paragraph 17), further comprising enabling the comparator upon the occurrence

of a signal that indicates that valid prefetch address data exists upon completion of a prefetch operation (column 6, lines 15-31).

19. **With respect to claim 10**, Watkins discloses an apparatus comprising:

- an address multiplexer (220 of Fig. 3) having a control input (POST_rd_addr/PF_addr of Fig. 3; column 3, lines 44-48); and
- an address comparator (316 of Fig. 2) having a received address input, a prefetched address input (column 6, lines 9-14), and an output coupled to the control input of the address multiplexer (indirectly through PF_HIT/MISS to State Machine 350 to POST_rd_addr/PF_addr of Fig. 3; column 3, lines 44-48).

20. **With respect to claim 11**, Watkins discloses an apparatus as defined in claim 10 (see above paragraph 19), wherein the address comparator output is coupled to assume a first value when the received address input is identical to the prefetched address input and to assume a second value when the received address input is not identical to the prefetched address input (column 6, lines 21-31).

21. **With respect to claim 12**, Watkins discloses an apparatus as defined in claim 11 (see above paragraph 20), wherein when the address comparator output is coupled to assume the first value, the address multiplexer is coupled to provide the prefetched address to the address multiplexer output (column 6, lines 27-31).

22. **With respect to claim 13**, Watkins discloses an apparatus as defined in claim 11 (see above paragraph 20), wherein when the address comparator output is coupled to assume the second value, the address multiplexer is coupled to provide the received address to the address multiplexer output (column 6, lines 27-31).

23. **With respect to claim 14**, Watkins discloses an apparatus as defined in claim 11 (see above paragraph 20), wherein the address comparator has an enable input to couple to a signal that assumes a predetermined enabled value when valid prefetched address data exists so that the address comparator is enabled only when valid prefetched address data is determined to exist at the address comparator prefetch address input (column 6, lines 15-31).

24. **With respect to claim 15**, Watkins discloses an apparatus as defined in claim 14 (see above paragraph 23), wherein when the address comparator output is coupled to assume the first value, the multiplexer is coupled to provide the prefetched address to the multiplexer output (column 6, lines 27-31).

25. **With respect to claim 16**, Watkins discloses an apparatus as defined in claim 14 (see above paragraph 23), wherein when the address comparator output is coupled to assume the second value the multiplexer is coupled to provide the received address to the multiplexer output (column 6, lines 27-31).

26. **With respect to claim 17**, Watkins discloses an apparatus as defined in claim 10 (see above paragraph 19), further comprising an address latch having a first input to accept a prefetched address, a second input to accept a received address, and an address output coupled to the received address input of the multiplexer to provide the received address to the multiplexer (column 6, lines 9-14; although a latch is not explicitly recited, the address bits must be stored in the multiplexer so that one address or the other can be output, so the multiplexer has the functional equivalent of a latch inside of it).

27. **With respect to claim 27**, Watkins discloses an article comprising a machine-readable medium containing instructions that, if executed, enable a system to determine whether a prefetched address is identical to a received address (abstract, lines 4-11; although this is a method, it could be implemented using code).

28. **With respect to claim 28**, Watkins discloses an article as defined in claim 27 (see above paragraph 27) further comprising instructions that, if executed, enable the system to apply a received address to a memory and to interrupt data transfer from the memory if the prefetched address is not identical to the received address (column 6, lines 27-31).

29. **With respect to claim 29**, Watkins discloses an article as defined in claim 28 (see above paragraph 28) further comprising instructions that, if executed, enable the system to compare the prefetched address and the received address when prefetching a respective prefetched address has been accomplished (the specification of the applicant notes, "Operation of COMPARE 22 is gated in the sense that its PFHIT output will be active only if the requisite PFVALID signal exists;" column 6, lines 15-31 of Watkins detail how the PFvalid signal will indicate a match, or become active, only when the PFvalid signal is active).

30. **With respect to claim 30**, Watkins discloses an article as defined in claim 29 (see above paragraph 29) further comprising instructions that, if executed enable the system to select an address to be applied to the memory synchronously with a system clock (column 3, lines 35-41 imply that the system can operate even if two components

in the system are using clocks with different frequencies, so therefore it could work using a single clock frequency).

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. **Claims 21-24** are rejected under 35 U.S.C. 103(a) as being anticipated over Watkins (US 5,854,911) in view of Kadi (US 2004/0117556).

33. **With respect to claim 21**, Watkins discloses

- A dynamic prefetch circuit coupled to a memory, the dynamic prefetch circuit comprising:
  - o an address multiplexer (220 of Fig. 3) having a control input (POST_rd_addr/PF_addr of Fig. 3; column 3, lines 44-48); and
  - o an address comparator (316 of Fig. 2) having a received address input, a prefetched address input (column 6, lines 9-14), and an output couple to the control input of the address multiplexer (indirectly through PF_HIT/MISS to State Machine 350 to POST_rd_addr/PF_addr of Fig. 3; column 3, lines 44-48).

Watkins does not disclose the limitation wherein there is

- an antenna coupled to the dynamic prefetch circuit.

However, Kadi discloses

- an antenna coupled to the dynamic prefetch circuit (270 of Figs. 5 and 6) [0036, line 4].

Watkins and Murakami et al. are analogous art because they are from the same field of endeavor, namely digital systems with data prefetching capabilities.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply the antenna of Kadi to the prefetch address checking system of Watkins. The motivation for doing so would have been to allow for "storage and/or retrieval of memory data provided over an air interface to the wireless communication device" [0036, lines 11-13].

Therefore, it would have been obvious to combine Kadi with Watkins for the benefit of a wireless device with an instruction prefetch address checking system to obtain the invention as specified in claim 21.

34. **With respect to claim 22**, Watkins and Kadi disclose a system as defined in claim 21 (see above paragraph 33); Watkins further distinguishes over claim 21 wherein the address comparator output is coupled to assume a first value when the received address input is identical to the prefetched address input and to assume a second value when the received address input is not identical to the prefetched address input (column 6, lines 21-31).

35. **With respect to claim 23**, Watkins and Kadi disclose a system as defined in claim 22 (see above paragraph 33); Watkins further distinguishes over claim 22 wherein

when the comparator is coupled to assume the first value, the multiplexer is coupled to provide the prefetched address to the multiplexer output (column 6, lines 27-31).

36. **With respect to claim 24**, Watkins and Kadi disclose a system as defined in claim 21 (see above paragraph 33); Watkins further distinguishes over claim 21 wherein the dynamic prefetch circuit further comprises an address latch, wherein the address latch comprises: a first address input to couple to a prefetched address generator; a second address input to couple to a source of received address; and an address output coupled to a received address in put of the address multiplexer (column 6, lines 9-14; although a latch is not explicitly recited, the address bits must be stored in the multiplexer so that one address or the other can be output, so the multiplexer has the functional equivalent of a latch inside of it).

Allowable Subject Matter

37. **Claims 18-20 and 25-26** objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

38. **With respect to claim 18**, the claim limitations are deemed allowable over the prior art of record as the prior art neither anticipates nor renders obvious at least the

combination with the inclusion in the claims "wherein the address latch has an output coupled to an enable input of the address comparator."

39. **With respect to claim 19**, the claim limitations are deemed allowable over the prior art of record as the prior art neither anticipates nor renders obvious the combination with the inclusion in the claims "wherein the address multiplexer has a… second address output coupled to the prefetched address input of the comparator."

40. **With respect to claim 20**, the claim limitations are deemed allowable over the prior art of record as the prior art neither anticipates nor renders obvious the combination of claim 19, upon which claim 20 is dependent.

41. **With respect to claim 25**, the claim limitations are deemed allowable over the prior art of record as the prior art neither anticipates nor renders obvious at least the combination with the inclusion in the claims "wherein the address latch further comprises: A PFDONE input to receive a signal that indicates that valid prefetched address data exists at the first address input of the address latch."

42. **With respect to claim 26**, the claim limitations are deemed allowable over the prior art of record as the prior art neither anticipates nor renders obvious the combination with the inclusion in the claims "wherein the address multiplexer has an output coupled to the prefetched address input of the comparator."

Conclusion

43. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Gonzales et al. (US 6,453,388) discloses a dynamic prefetch system.

- Moyer et al. (US 2005/0132173) discloses a logic circuit very similar to that found in claims 18-20.
- Sunaga et al., "A Full Bit Prefetch Architecture for Synchronous DRAM's," in *IEEE Journal of Solid State Circuits*, Volume 30, Issue 9, September 1995.

44. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James R. Golden whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James R. Golden
Patent Examiner
Art Unit 2187

12/01/2005

Brian R. Peugh
Primary Examiner
AU 2187